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DATA SHEET

SAA5250
Interface for data acquisition and control
(for multi-standard teletext systems)

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Interface for data acquisition and control (for multi-standard teletext systems)

SAA5250

GENERAL DESCRIPTION

The SAA5250 is a CMOS Interface for Data Acquisition and Control (CIDAC) designed for use in conjunction with the Video Input Processor (SAA5230) in a multi-standard teletext decoder. The device retrieves data from a user selected channel (channel demultiplexer), as well as providing control signals and consecutive addressing space necessary to drive a 2 K bytes buffer memory.

The system operates in accordance with the following transmission standards:

- French Didon Antiope specification D2 A4-2 (DIDON)
- North American Broadcast Teletext specification (NABTS)
- U.K. teletext (CEEFAX)

Features

- 7,5 MHz maximum conversion rate
- Three prefixes; DIDON, NABTS and U.K. teletext (CEEFAX)
- Mode without prefix
- Internal calculation of the validation (VAL) and colour burst blanking (CBB) signals, if programmed
- Programmable framing code and channel numbers
- Error parity calculation or not (odd parity)
- Hamming processing of the prefix byte
- Full channel or VBI reception
- Slow/fast mode (detection of page flags or not)
- Maximum/default format up to 63 bytes
- Addressing space of 2 K bytes of the static memory
- Multiplexed address/data information is compatible with Motorola or Intel microcontrollers
- CIDAC is ‘MOTEL’ compatible

PACKAGE OUTLINES

SAA5250P: 40-lead DIL; plastic (SOT129); SOT129-1; 1996 December 02.
SAA5250T: 40-lead mini-pack; plastic (VSO40); SOT158-1; 1996 December 02.

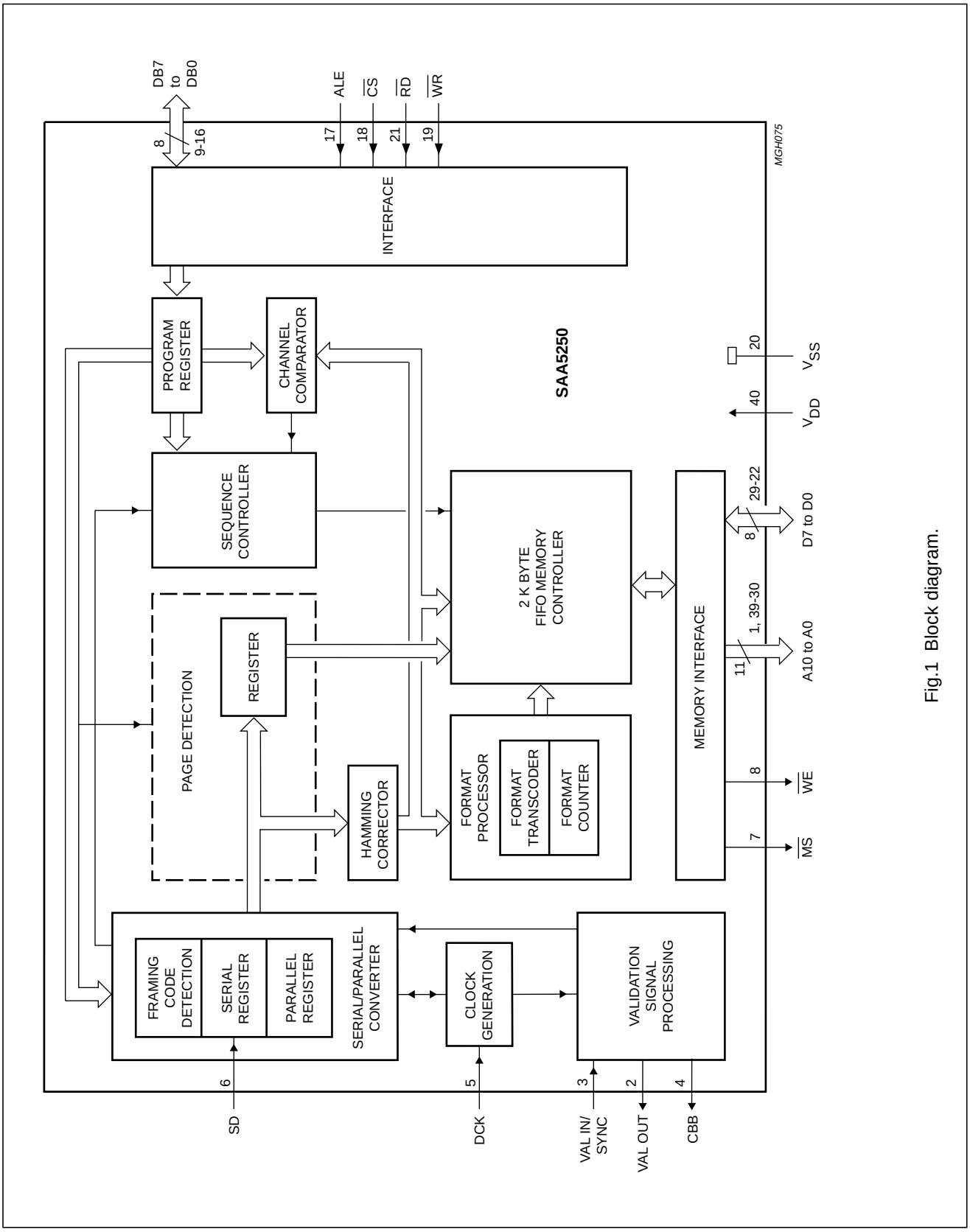


Fig.1 Block diagram.

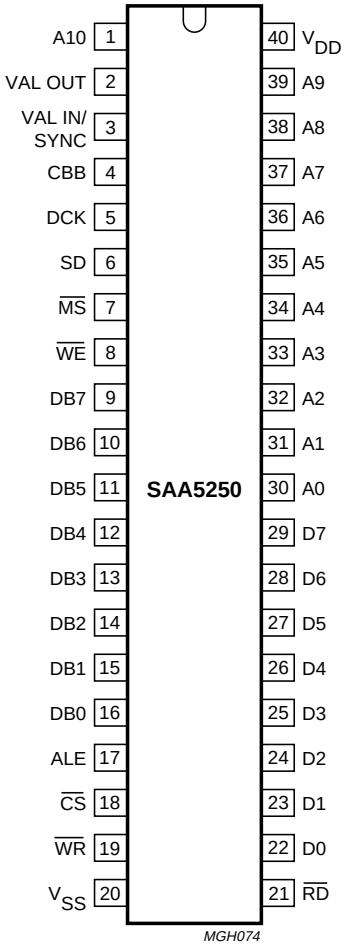


Fig.2 Pinning diagram.

PINNING FUNCTION

MNEMONIC	PIN NO.	FUNCTION
A10 and A0 to A9	1 and 30 to 39	Memory address outputs used by CIDAC to address a 2 K byte buffer memory
VAL OUT	2	Validation output signal used to control the location of the window for the framing code.
VAL IN/SYNC	3	Validation input signal (line signal) used to give or calculate a window for the framing code detection
CBB	4	Colour burst blanking output signal used by the SAA5230 as a data slicer reset pulse
DCK	5	Data clock input, in synchronization with the serial data signal
SD	6	Serial data input, arriving from the demodulator
$\overline{MS}$	7	Chip enable output signal for buffer memory selection
$\overline{WE}$	8	Write command output for the buffer memory
DB7 to DB0	9 to 16	8-bit three state input/output data/address bus used to transfer commands, data and status between the CIDAC registers and the CPU
ALE	17	Demultiplexing input signal for the CPU data bus
$\overline{CE}$	18	Chip enable input for the SAA5250
$\overline{WR}$	19	Write command input (when LOW)
V_{SS}	20	ground
$\overline{RD}$	21	Read command input (when LOW)
D0 to D7	22 to 29	8-bit three state input/output data bus used to transfer data between CIDAC and the buffer memory
V_{DD}	40	+5 V power supply

FUNCTIONAL DESCRIPTION

Microcontroller interface

The microcontroller interface communicates with the CPU via the handshake signals DB7 – DB0, ALE, CS, $\overline{RD}$, $\overline{WR}$. The microcontroller interface produces control commands as well as programming the registers to write their contents or read incoming status/data information from the buffer memory. The details of the codes used to address the registers are given in Table 2.

The CIDAC is 'MOTEL' compatible (MOTEL compatible means it is compatible with standard **Mo**torola or In**tel** microcontrollers). It automatically recognizes the microcontroller type (such as the 6801 or 8501) by using the ALE signal to latch the state of the $\overline{RD}$ input. No external logic is required.

Table 1 Recognition signals

CIDAC	8049/8051 TIMING 1	6801/6805 TIMING 2
ALE	ALE	AS
$\overline{RD}$	$\overline{RD}$	DS, E, Φ 2
$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$

Table 2 CIDAC register addressing

CODES						FUNCTION
R	W	CS	DB2	DB1	DB0	
1	0	0	0	0	0	write register R0
1	0	0	0	0	1	write register R1
1	0	0	0	1	0	write register R2
1	0	0	0	1	1	write register R3
1	0	0	1	0	0	write register R4
1	0	0	1	0	1	write register R5
1	0	0	1	1	0	write command register R6 (initialization command)
1	0	0	1	1	1	write register R7
0	1	0	0	0	0	read status
0	1	0	0	0	1	read data register
0	1	0	0	1	0	test (not used)
0	1	0	0	1	1	test (not used)

Register organization

R0 register

Table 3 R0 Register contents

R04 SLOW/FAST MODE	R03 PARITY	R02 TO R00 USED PREFIXES
0 = slow mode	0 = no parity control	000 = DIDON long
1 = fast mode	1 = odd parity	001 = DIDON medium
		010 = DIDON short
		011 = not used
		100 = U.K. teletext
		101 = NABTS
		110 = without prefix
		111 = without prefix

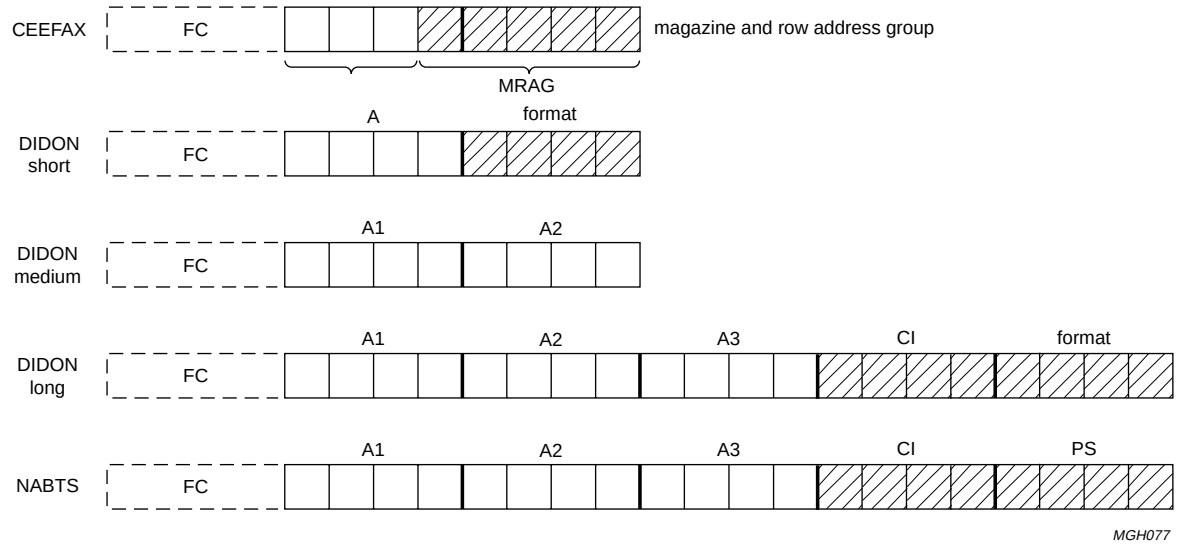


Fig.3 Five prefixes.

All of the bytes (see Fig.3) are Hamming protected. The hatched bytes are always stored in the memory in order to be processed by the CPU (see section ‘Prefix processing’). In the mode without prefix all of the bytes which follow the framing code are stored in the memory until the end of the data packet, the format is then determined by the contents of the R3 register.

If R03 = 0; no parity control is carried out and the 8-bits of the incoming data bytes are stored in the fifo memory.

If R03 = 1; the 8th bit of the bytes following the prefix (data bytes) represents the result of the odd parity control.

If R04 = 0; the device operates in the slow mode. The CIDAC retrieves data from the user selected magazine (see section ‘R1 and R2’) and without searching for a start to a page stores the data into the FIFO memory.

If R04 = 1; the device operates in the fast mode. Prior to writing into the FIFO memory, the CIDAC searches for a start to a page which is variable due to the different prefixes:

- DIDON (long, medium and short): using the redundant bytes, SOH RS, X RS and SOH X (where X is a bit affected by a parity error)
- NABTS, the least significant bit of the PS byte is set to 1
- U.K. teletext, ROW = 0

R1 register

Table 4 R1 Register contents

R17 **VAL IN/SYNC**	**R16 TO R14** **FORMAT TABLE** (1)	**R13 TO R10** **CHANNEL NUMBERS (FIRST DIGIT)**
1 = VAL 0 = SYNC	000 = list 1 001 = list 2 010 = list 3 011 = list 4 1XX = maximum/default value used (R3)	first digit hexadecimal value

Note

1. X = don't care

If VAL IN/SYNC = 1; the line signal immediately produces a validation signal for the framing code detection.

If VAL OUT = 0; the line signal is used as a starting signal for an internally processed validation signal (see Fig.15). The framing code window width is fixed at 13 clock periods and the delay is determined by the contents of the R5 register (R56 to R50).

At any moment the user is able to ensure that the framing code window is correctly located. This is accomplished by the VAL OUT pin reflecting the internal validation signal. A CBB signal with programmable width (see section 'R7 register') can also be generated, this is used as a data slicer reset pulse by the SAA5230. The line signal is used as the starting point of the internal CBB signal width fixed by the contents of the R7 register.

If R16 = 0; then bits R15 and R14 provide the format table number using DIDON long and short prefixes (see Table 6).

If R16 = 1; then the format is determined by the contents of the R3 register.

The bits R13 to R10 represent the first channel number to be checked in the prefix. In U.K. teletext mode only 3 bits are required, so R13 = X.

Table 5 Format table

FORMAT BYTE B8, B6, B4 AND B2 (1)	LIST 1	LIST 2	LIST 3	LIST 4
0000	0	0	0	0
0001	1	1	1	1
0010	2	2	2	2
0011	3	3	3	3
0100	4	5	6	7
0101	8	9	10	11
0110	12	13	14	15
0111	16	17	18	19
1000	20	21	22	23
1001	24	25	26	27
1010	28	29	30	31
1011	32	33	34	35
1100	36	37	38	39
1101	40	41	42	43
1110	44	45	46	47
1111	48	49	50	51

Note

1. B8 = MSB and B2 = LSB.

R2 register

Table 6 R2 Register contents

R27 TO R24	R23 TO R20
channel number, third digit	channel number, second digit
(hexadecimal value, third digit)	(hexadecimal value, second digit

Note

1. R27 and R23 = MSB and R24 and R20 = LSB

The R2 register provides the other two parts of the channel number (depending on the prefix) that require checking.

R3 register

Table 7 R3 register contents

	R35 TO R30 6-BIT FORMAT MAXIMUM/DEFAULT VALUE
	000000 = 0 000001 = 1 – – – 111111 = 63

This 6-bit byte gives:

- In the DIDON long and short mode, a maximum format in case of corrupted transmission (multiple errors on the Hamming corrector)
- A possible 63-bit format for all types of prefix

R4 register

Table 8 R4 register contents

	R47 TO R40
	8-bit register used for storing the framing code value which will be compared with the third byte of each data line

R5 register

Table 9 R5 register contents

	R57 NEGATIVE/POSITIVE		**R56 TO R50 SYNCHRONIZATION DELAY**
	0 = negative edge for sync signal 1 = positive edge for sync signal		7-bit sync delay, giving a maximum delay of $(2^7 - 1) \times 10^6$ µs/F (Hz)

Note

1. F = data clock acquisition frequency (DCK).

Using R57 it is possible to start the internal synchronization delay (t_{DVAL}) on the positive or negative edge.

R6 write command register

This is a fictitious register. Only the address code (see Table 2) is required to reset the CIDAC. See Table 11 for the status of the FIFO memory on receipt of this command.

R7 register

Table 10 R7 register contents

	R75 TO R70
	6-bit register used to give a maximum colour burst blanking signal of: $(2^6 - 1) \times 10^6$ µs/F (Hz)

Note

1. F = data clock acquisition frequency.

*Fifo status register (*read R0 register)

Table 11 Fifo register contents

DB2 TO DB0		
DB2 = 1 memory empty	DB1 = 1, data not present in the read data register	DB0 = 0 memory not full

Once the relevant prefix and the right working modes have been given by the corresponding registers, a write command to the R6 register enables the CIDAC to accept and process serial data.

Channel comparator

This is a four bit comparator which compares the three user hexadecimal defined values in R1 and R2 to corresponding bytes of the prefix coming from the Hamming corrector. If the three bytes match, the internal process of the prefix continues. If they do not match the CIDAC returns to a wait state until the next broadcast data package is received.

FIFO memory controller

The FIFO memory contains all the necessary functions required for the control of the 11-bit address memory (2 K byte). The functions contained in the FIFO memory are as follows:

- write address register (11-bits)
- read address register (11-bits)
- memory pointer (11-bits)
- address multiplexer (11-bits)
- write data register (8-bits)
- read data register (8-bits)
- data multiplexer
- control logic

The FIFO memory provides the memory interface with the following:

- 11-bit address bus (A10 to A0)
- 8-bit data bus (D7 to D0)
- two control signals, memory select ($\overline{MS}$) and write enable ($\overline{WE}$)

Operation

The CIDAC uses the same clock signal for data acquisition and internal processing, this allows the CIDAC to have a write and a read cycle during each character period (see Fig.13). The first half of the character period is a write cycle and the second half is a read cycle. Consequently, for an 8 MHz bit rate the maximum memory cycle time is 500 ns.

When the first data byte is written into the FIFO memory, thus transferred into the read register, the FIFO memory enters the status shown in Table 12.

Table 12 FIFO status

DB2 TO DB0		
DB2 = 1 memory empty	DB1 = 0 data available	DB0 = 0 memory not full

When the FIFO memory is full two events occur:

- the write address register points to the next address after the last written address
- when new data is to be written, the memory select signal output ceases

Memory interface

The memory interface contains all the buffers for the memory signals mentioned in the section ‘FIFO memory controller’.

Page detection

This part of the CIDAC contains a parallel register with logic which detects (only in fast mode) a start of a page or data group (see section ‘R0 register’).

Hamming correction (see Tables 13 and 14)

The Hamming correction provides (see section ‘Prefix processing’):

- hexadecimal value of the Hamming code
- accept/reject code signal
- parity information

Table 13 Hamming correction (coding)

HEXADECIMAL NOTATION	B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	1
3	0	1	0	1	1	1	1	0
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	0	1	1
6	0	0	1	1	1	0	0	0
7	0	0	1	0	1	1	1	1
8	1	1	0	1	0	0	0	0
9	1	1	0	0	0	1	1	1
A	1	0	0	0	1	1	0	0
B	1	0	0	1	1	0	1	1
C	1	0	1	0	0	0	0	1
D	1	0	1	1	0	1	1	0
E	1	1	1	1	1	1	0	1
F	1	1	1	0	1	0	1	0

Note

1. $B7 = B8 \oplus B6 \oplus \overline{B4}$
   $B5 = B6 \oplus \overline{B4} \oplus \overline{B2}$
   $B3 = \overline{B4} \oplus \overline{B2} \oplus B8$
   $B1 = \overline{B2} \oplus B8 \oplus B6$
   $\oplus$ = exclusive OR gate function
   B8, B6, B4 and B2 = data bits
   B7, B5, B3 and B1 = redundancy bits

Table 14 Hamming correction (decoding)

A	B	C	D	INTERPRETATION	INFORMATION
1	1	1	1	no error	accepted
0	0	1	0	error on B8	corrected
1	1	1	0	error on B7	accepted
0	1	0	0	error on B6	corrected
1	1	0	0	error on B5	accepted
1	0	0	0	error on B4	corrected
1	0	1	0	error on B3	accepted
0	0	0	0	error on B2	corrected
0	1	1	0	error on B1	accepted
A.B.C = 0			1	multiple errors	rejected

Note

1. A = B8 ⊕ B6 ⊕ B2 ⊕ B1
   B = B8 ⊕ B4 ⊕ B3 ⊕ B2
   C = B6 ⊕ B5 ⊕ B4 ⊕ B2
   D = B8 ⊕ B7 ⊕ B6 ⊕ B5 ⊕ B4 ⊕ B3 ⊕ B2 ⊕ B1
   ⊕ = exclusive OR gate function

Format processing

The format processing consist of two parts:

part 1

A format transcoder produces a 6-bit code (up to 63) and uses the following as inputs:

- DIDON long and short prefixes;
  hamming corrected code (4-bits)
  accept/reject code condition
  table number (see section ‘R1 register’, bits R15 and R14)
- Other prefixes (R16 = 1)
- 6-bit maximum/default format (see section ‘R3 register’)

part 2

A format counter operating at the character clock frequency which receives the 6-bit code from the format transcoder and is used to check the data packet length following the prefix.

Serial/parallel converter

The serial/parallel converter consists of three parts:

- An 8-bit shift register which receives the SD input and operates at the bit frequency (DCK).
- An 8-bit parallel register used for storage.
- A framing code detection circuit. This logic circuit compares the 8-bits of the R4 register with that of the serial register. If seven bits out of eight match (in coincidence with a validation window), it produces a start signal for a new teletext data line to the sequence controller.

Clock generation

The clock generator does the following:

- acts as a buffer for the DCK clock
- generates the character clock

As soon as a framing code has been detected, a divide by 8 counter is initialized and the character clock is started. The clock drives the following:

- sequence controller
- parallel registers
- format counter

Processing of VAL and CBB signals

The circuit has one input (VAL IN/SYNC) and two outputs (VAL OUT and CBB). The circuit consists of:

- 7-bit counter operating at DCK frequency which produces the framing code validation pulse delay
- 7-bit comparator which compares the contents of the R5 register (bits R56 to R50) to the bit counter
- a 6-bit counter operating at DCK frequency which produces the CBB pulse width
- 6-bit comparator which compares the contents of the R7 register (bits R75 to R70) to the bit counter
- control logic required to provide the start condition for the VAL signal and the CBB pulse width (on the negative or positive edge of the sync signal)

The CBB signal useful occurs when the associated video processor:

- has no sandcastle pulse to send back to the demodulator
- carries out the synchronization of the time base clock. In this event the CBB acts as a data slicer reset pulse

The VAL OUT is a control signal which reflects the internal framing code window.

Prefix processing (see Table 21)

Figs 4 to 9 show the acquisition flow charts for each prefix type coded in the R0 register (bits R02 to R00).

As soon as an initialization command is received by the CIDAC, a write command to the R6 register (only the address is significant), is ready to receive data from a dedicated channel number and store the data in the FIFO memory (explained in the following paragraphs, each paragraph being dedicated to an individual type of prefix).

DIDON long (see Fig.4)

In this mode, the continuity index, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 15 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 16 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

Note

1. A/R = 0, if rejected
2. A/R = 1, if accepted
3. X = don’t care

DIDON mediun (see Fig.5)

Only data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

DIDON short (see Fig.6)

In this mode, format and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFIFO memory only after a page detection.)

Table 17 Format processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	F5	F4	F3	F2	F1	F0

NABTS (see Fig.7)

In this mode, the continuity index, packet structure and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a page detection.)

Table 18 Continuity index processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	CI3	CI2	CI1	CI0

Table 19 Packet structure processing result

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	X	PS3	PS2	PS1	PS0

U.K. teletext (see Fig.8)

In this mode, the magazine and row address group (two bytes) and data bytes are written into the FIFO memory. (In fast mode, information can be written into the FIFO memory only after a flag detection.)

Table 20 Magazine and row address group processing results

D7	D6	D5	D4	D3	D2	D1	D0
A/R	X	X	RW4	RW3	RW2	RW1	RW0

Without prefix

All the data following the framing code are stored in the FIFO memory.

Table 21 Prefix processing

PREFIXES	CONSTRUCTION OF PREFIXES	BYTES STORED IN FIFO MEMORY DURING SLOW MODE	BYTES STORED IN FIFO MEMORY DURING FAST MODE
DIDON long	A1, A2, A3, CI, F and D	CI, F and D	CI(1) , F(1) and D(1)
DIDON medium	A1, A2 and D	D	D(1)
DIDON short	A1, F and D	F and D	F(1) and D(1)
NABTS	A1, A2, A3 CI, PS and D	CI, PS and D	CI(1), PS(1) and D(1)
U.K. teletext	MRAG and D	MRAG and D	MRAG(1) and D(1)
without prefix		all bytes of the data packet following the framing code are written into the FIFO memory	

Note

1. after page/flag detection
2. A1, A2, A3 are channel numbers
   CI = continuity index
   F = format
   PS = packet structure
   D = data
   MRAG = magazine and row address group

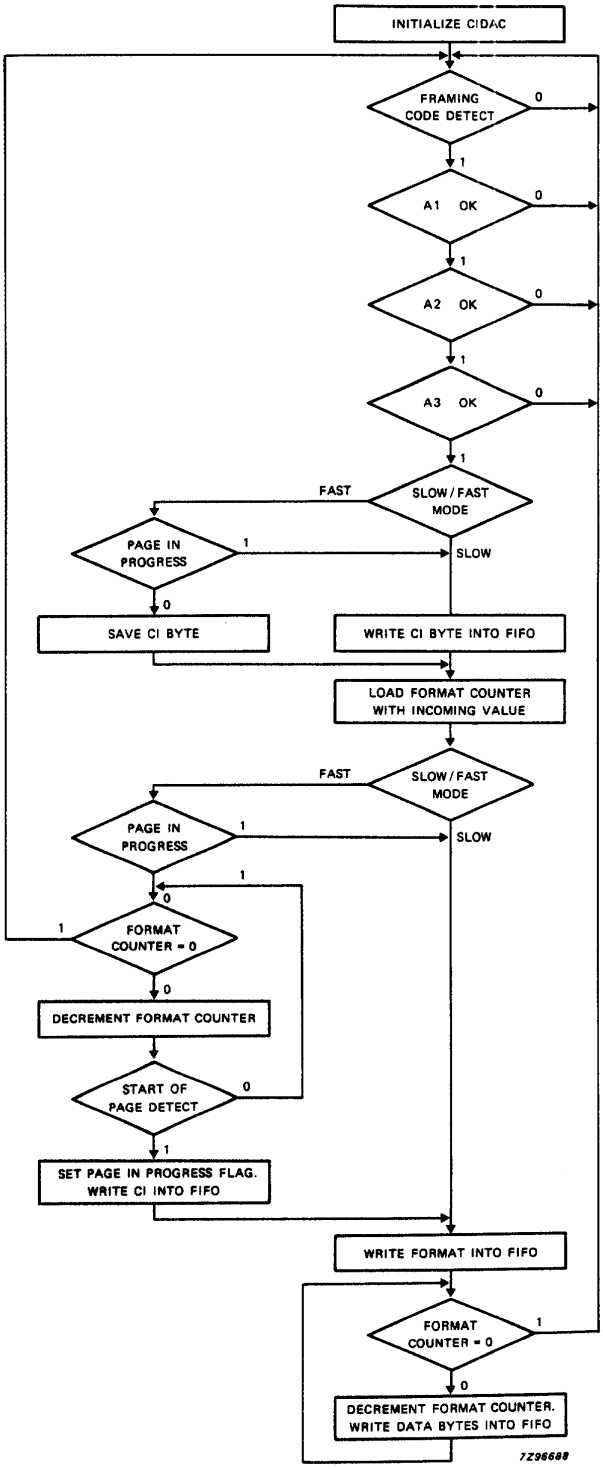


Fig.4 DIDON (long) acquisition flow chart.

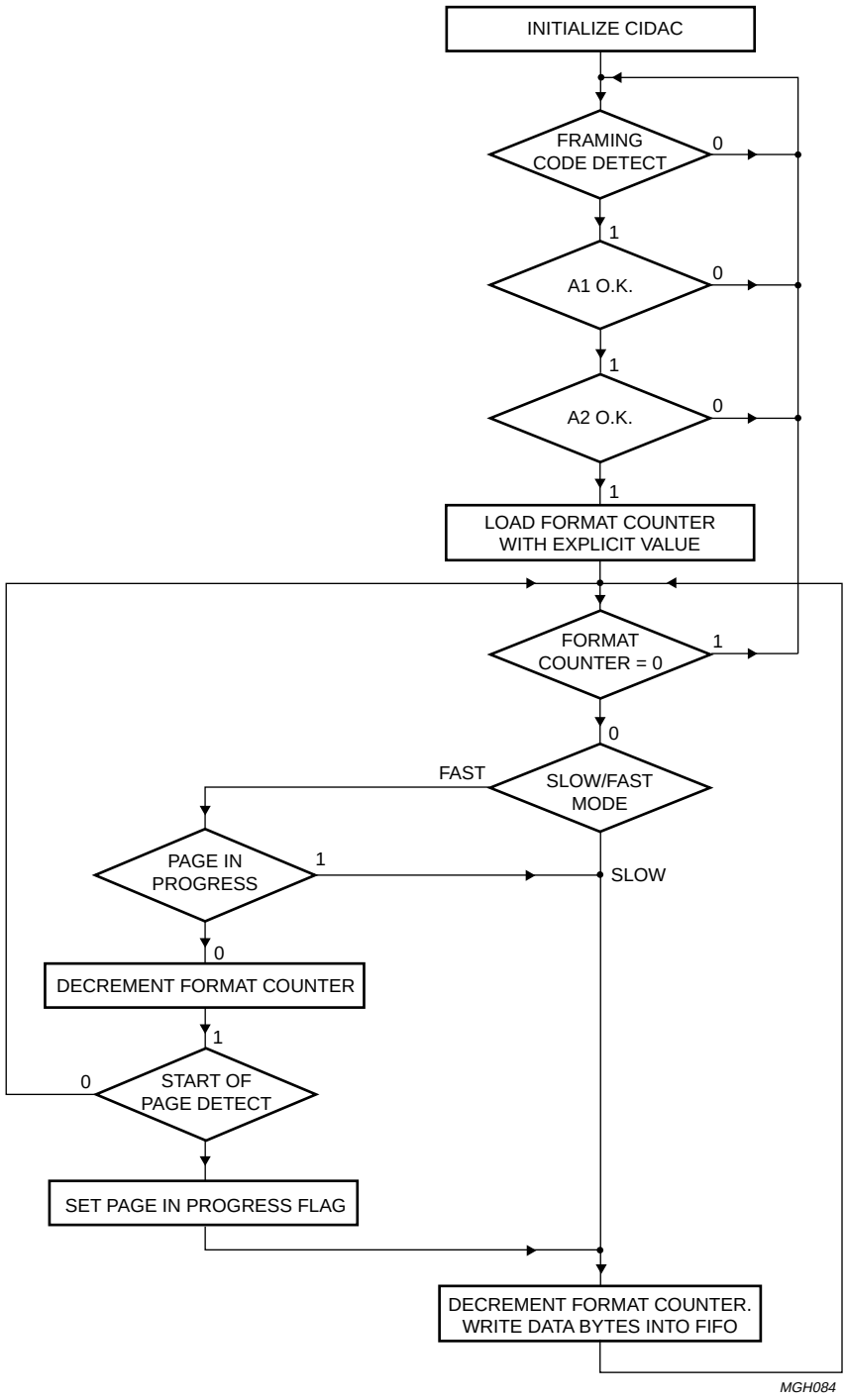


Fig.5 DIDON (medium) acquisition flow chart.

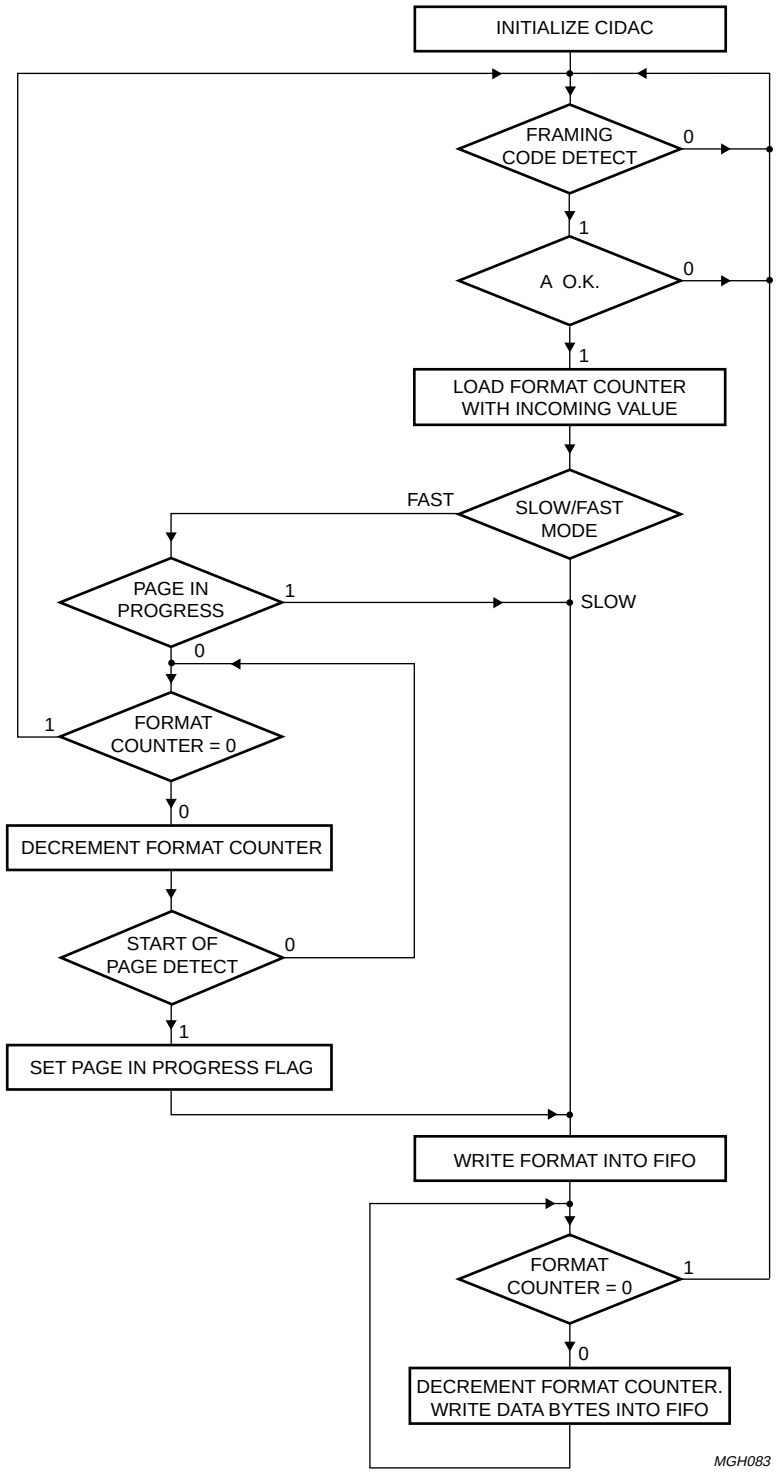


Fig.6 DIDON (short) acquisition flow chart.

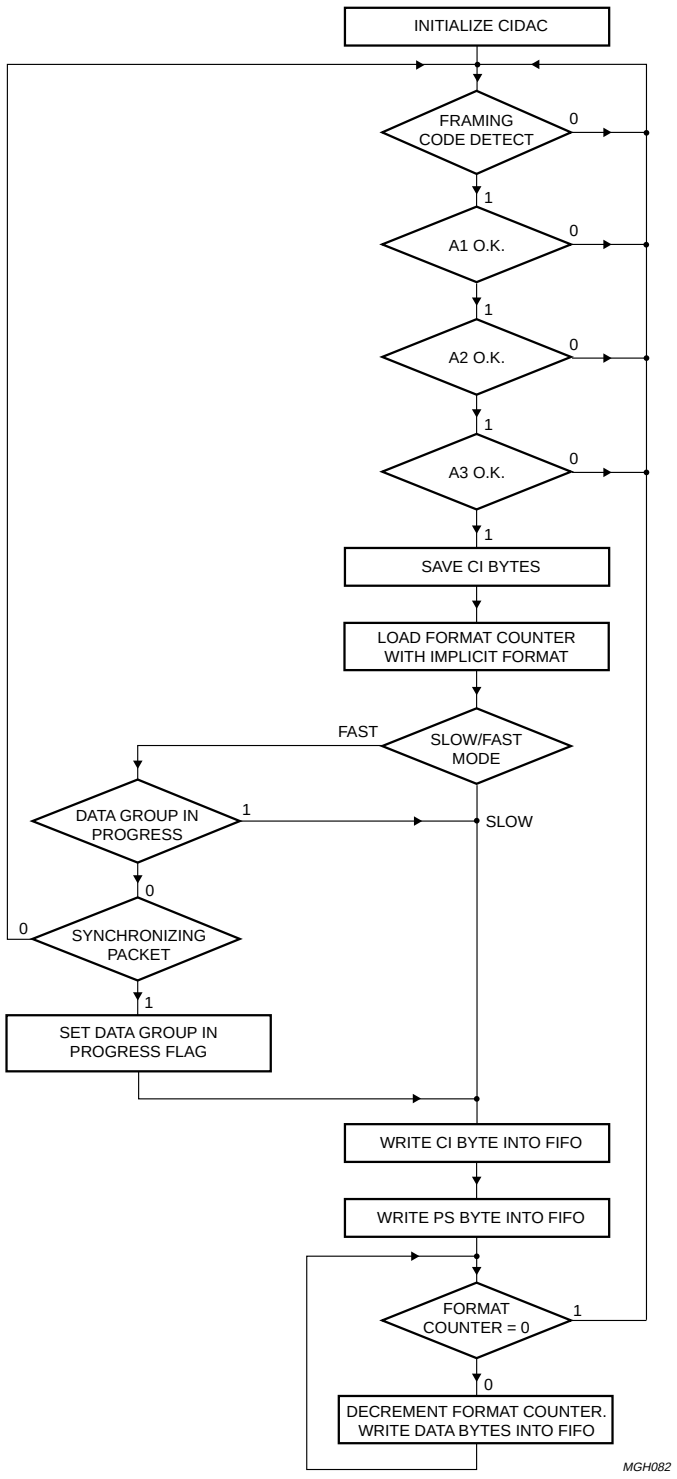


Fig.7 NABTS acquisition flow chart.

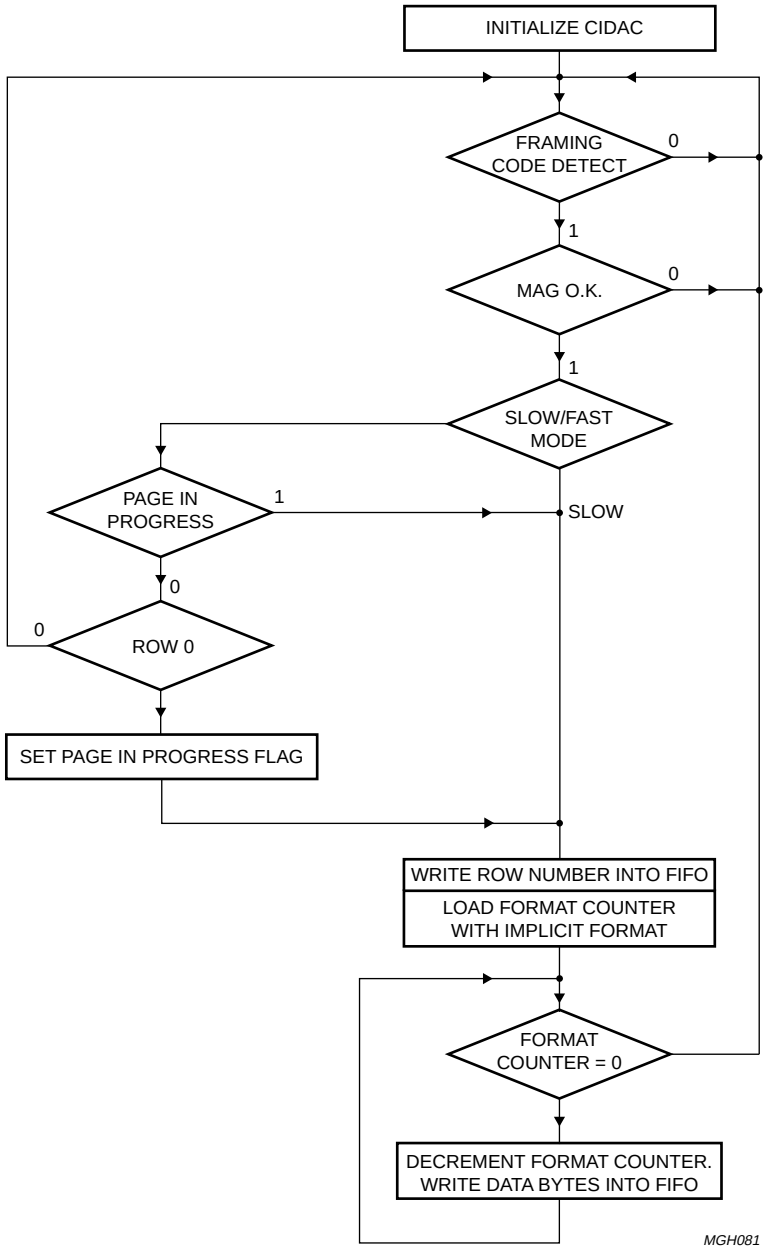


Fig.8 U.K. teletext acquisition flow chart.

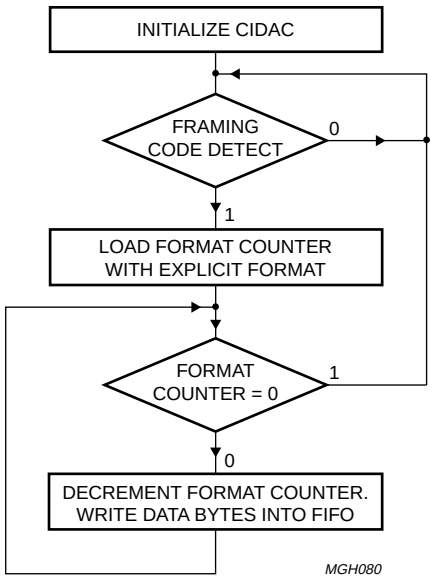


Fig.9 Without prefix acquisition chart.

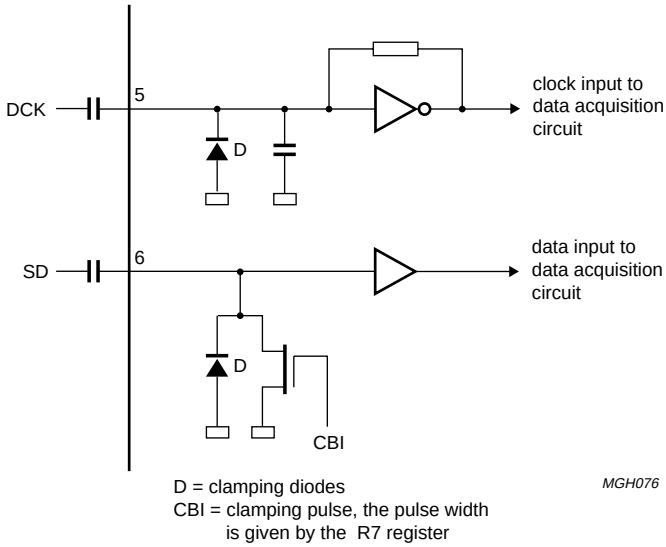


Fig.10 SD and DCK input circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range		V_{DD}	–0,3	6,5	V
Input voltage range		V_I	–0,3	V_{DD}+0,3	V
Total power dissipation		P_{tot}	–	400	mW
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	–20	+125	°C

D.C. CHARACTERISTICS (except SD and DCK)

V_{DD} = 5 V±10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range		V_{DD}	4,5	5,0	5,5	V
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input voltage LOW		V_{IL}	–	–	0,8	V
Input leakage current		I_I	–	–	1,0	µA
Output voltage HIGH	I_{load} = 1 mA	V_{OH}	V_{DD}–0,4	–	–	V
Output voltage LOW	I_{load} = 4 mA, at pins 9 to 16 and 22 to 29	V_{OL}	–	–	0,4	V
	I_{load} = 1 mA all other outputs	V_{OL}	–	–	0,4	V
Power dissipation		P	–	5	–	mW
Input capacitance		C_I	–	–	7,5	pF

SD and DCK D.C. CHARACTERISTICS (see Fig.10)

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 0 to 70 °C, unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DCK						
Input voltage range (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input current	V_I = 0 to V_{DD}	I_I	5	–	200	µA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{text}	10	–	–	nF
SD						
D.C. input voltage range HIGH	note 1	V_{IH}	2,0	–	–	V
D.C. input voltage range LOW	note 2	V_{IL}	–	–	0,8	V
A.C. input voltage (peak-to-peak value)		$V_{I(p-p)}$	2,0	–	–	V
Input leakage current	V_I = 0 to V_{DD}	I_I	–	–	10	µA
Input capacitance		C_I	–	–	30	pF
External coupling capacitor		C_{ext}	10	–	–	nF

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; Reference levels for all inputs and outputs, V_{IH} = 2 V; V_{IL} = 0,8 V; V_{OH} = 2,4 V; V_{OL} = 0,4 V; C_L = 50 pF on DB7 to DB0; T_{amb} = 0 to 70 = C, unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Microcontroller interface	Figs 11 and 12					
Cycle time		t_{CY}	400	–	–	ns
Address pulse width		t_{LHLL}	50	–	–	ns
$\overline{RD}$ HIGH or $\overline{WR}$ to ALE HIGH	Fig.11	t_{AHRD}	0	–	–	ns
DS LOW to AS HIGH	Fig.12	t_{AHRD}	0	–	–	ns
ALE LOW to $\overline{RD}$ LOW or $\overline{WR}$ LOW	Fig.11	t_{ALRD}	30	–	–	ns
AS LOW to DS HIGH	Fig.12	t_{ALRD}	30	–	–	ns
Write pulse width		t_{WL}	120	–	–	ns
Address and chip select set-up time		t_{ASL}	10	–	–	ns
Address and chip select hold time		t_{AHL}	20	–	–	ns
Read to data out period		t_{RD}	–	–	130	ns
Data hold after $\overline{RD}$		t_{DR}	10	–	100	ns
R/$\overline{W}$ to DS set-up time	Fig.12	t_{RWS}	40	–	–	ns
R/$\overline{W}$ to DS hold time	Fig.12	t_{RWH}	10	–	–	ns
Data set-up time	write cycle	t_{DW}	50	–	–	ns
Data hold time	write cycle	t_{WD}	10	–	–	ns
Read pulse width	note 3	t_{RL}	150 or DCK + 50	–	–	ns
Memory interface	Fig.13					
$\overline{WE}$ LOW to DCK falling edge		t_{WEL}	10	–	80	ns
$\overline{WE}$ HIGH to DCK falling edge		t_{WEH}	10	–	80	ns
$\overline{MS}$ LOW to DCK rising edge		t_{MSL}	10	–	80	ns
$\overline{MS}$ HIGH to DCK rising edge		t_{MSH}	10	–	85	ns
Address output from DCK rising edge		t_{AV}	10	–	120	ns
Data output from $\overline{WE}$ falling edge		t_{DWL}	0	–	10	ns
Data hold from $\overline{WE}$ rising edge		t_{DWH}	0	–	–	ns
Address set-up time to data	note 4	t_{AD}	–	–	3 × DCK –110	ns
$\overline{WE}$ pulse width	note 5	t_{WEW}	3 × DCK	–	–	ns
$\overline{MS}$ pulse width	note 6	t_{MSW}	2 × DCK	–	–	ns

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Demodulator interface						
(see SD and DCK D.C. CHARACTERISTICS)	Fig.14					
DCK LOW	conversion rate < 7,5 MHz	t_{DCKL}	55	–	–	ns
DCK HIGH	conversion rate < 7,5 MHz	t_{DCKH}	55	–	–	ns
Serial data set-up time		t_{SSD}	0	–	–	ns
Serial data hold time		t_{HSD}	30	–	–	ns
Validation signal set-up time		t_{SVALI}	50	–	–	ns
Validation signal hold time		t_{HVALI}	50	–	–	ns
Other I/O signals	Fig.15					
User definable width as a multiple of DCK period		t_{WCBB}	0	–	63	DCK
Validation signal width	note 7	t_{WVAL}	X	12	X	DCK
User definable delay as a multiple of DCK period		t_{DVAL}	0	–	127	DCK

Notes to the characteristics

1. Unless R7 = 00 the value given is unacceptable.
2. When CBI signal is maintained at 0 V (R7 = 00) and if SD input signal is correctly referenced to ground, no coupling capacitor is required.
3. DCK + 50 is the DCK period plus 50 ns.
4. 3 × DCK – 110 is 3 × DCK period – 110 ns.
5. 3 × DCK is 3 × DCK period.
6. 2 × DCK is 2 × DCK period.
7. X = irrelevant.

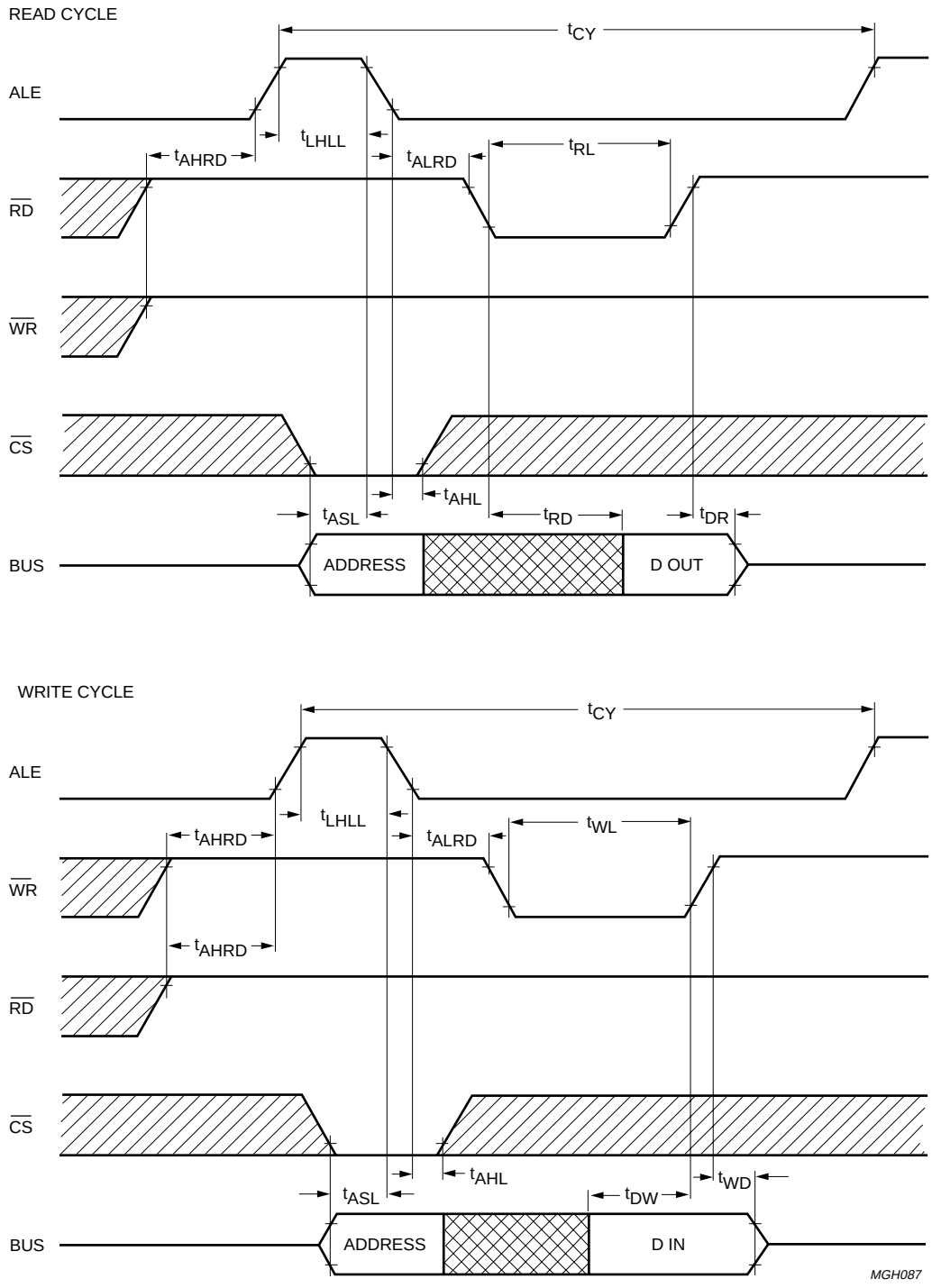


Fig.11 Timing diagram for microcontroller interface (Intel).

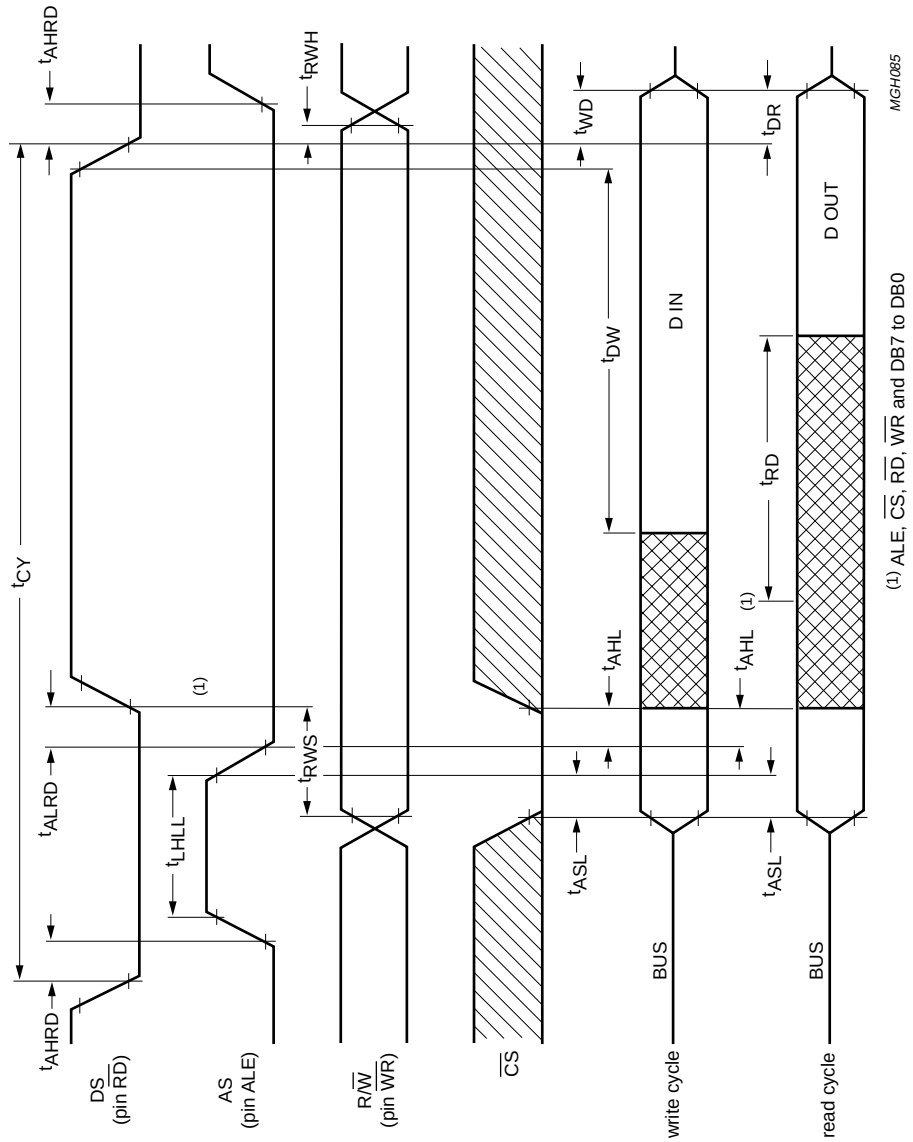


Fig.12 Timing diagram for microcontroller interface (Motorola).

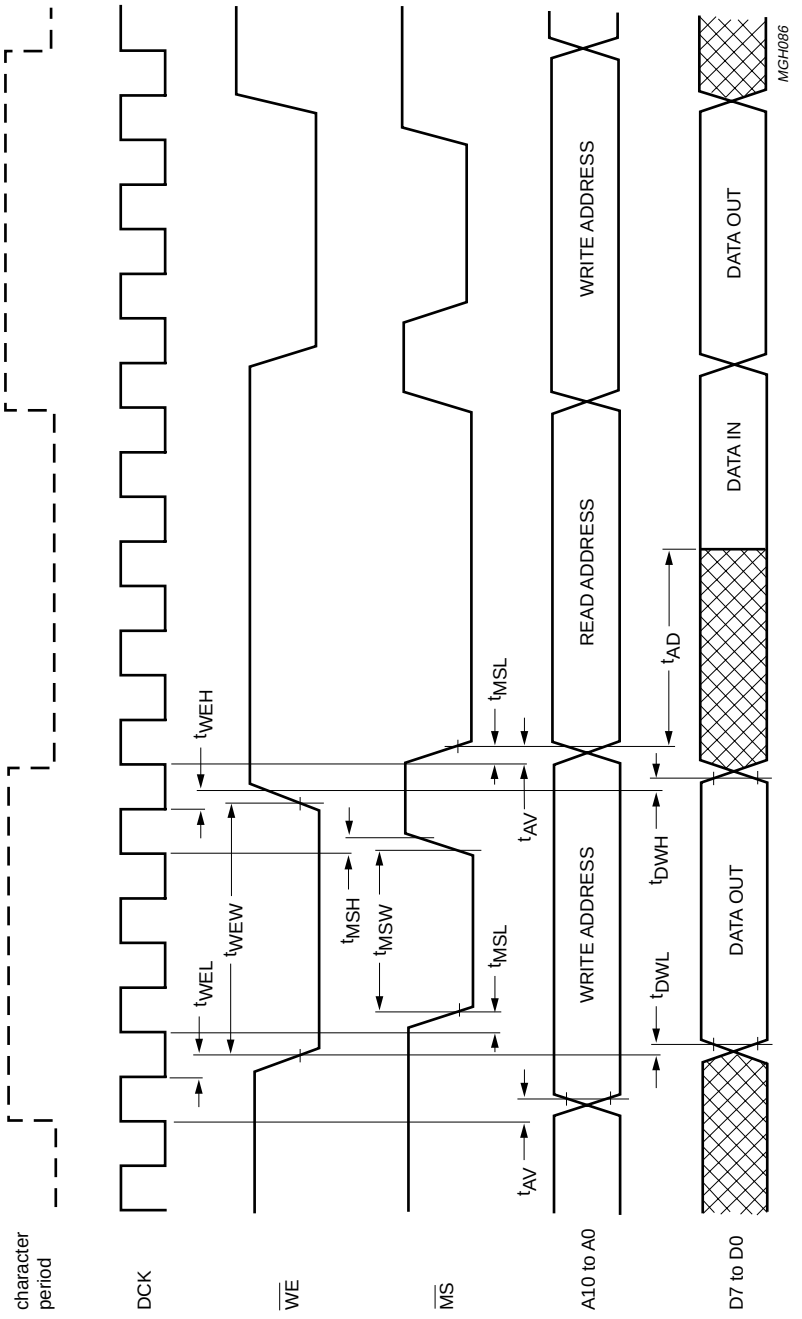


Fig.13 Timing diagram for memory interface.

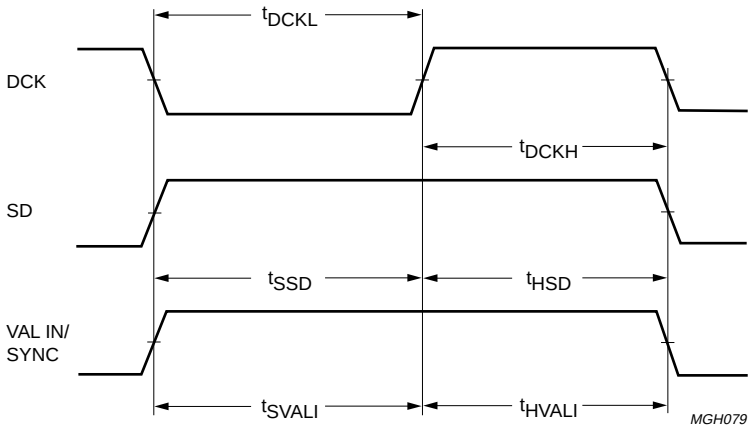


Fig.14 Timing diagram for demodulator interface.

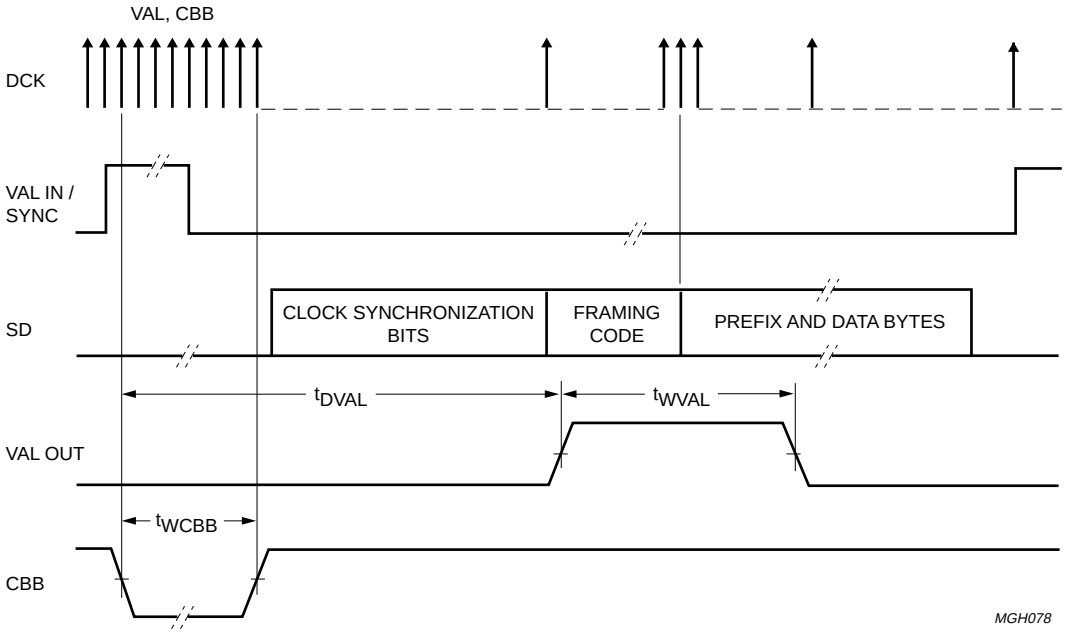
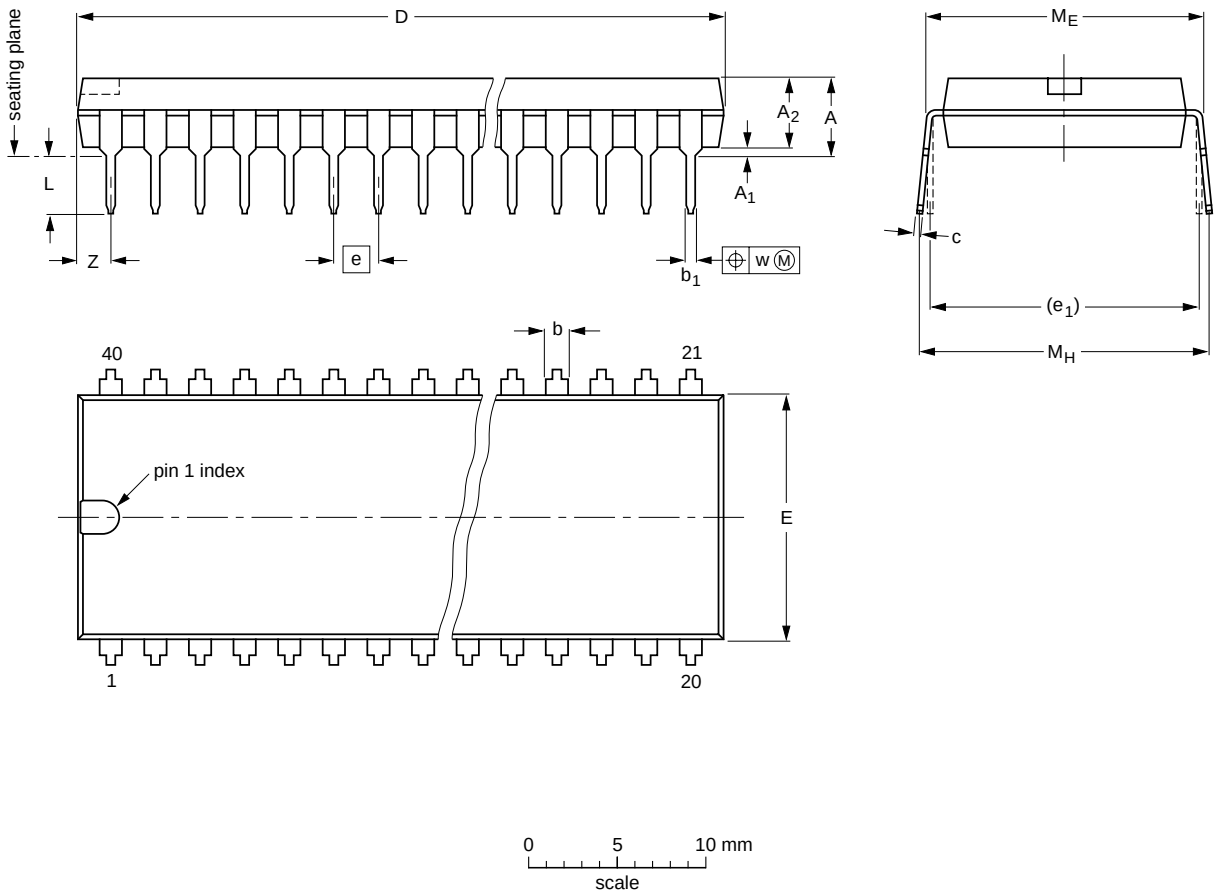


Fig.15 Timing diagram for all other I/O signals.

PACKAGE OUTLINES

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

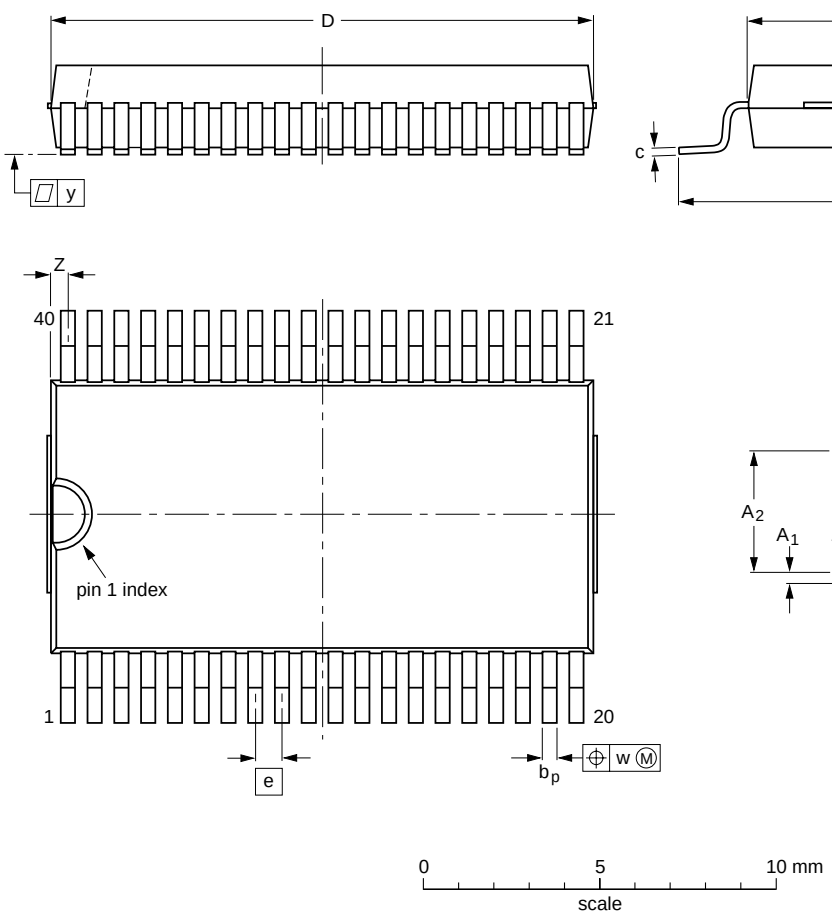
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7^o 0^o
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO and VSO

Reflow soldering

Reflow soldering techniques are suitable for all SO and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO and VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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